What is claimed is:

1. A nonvolatile semiconductor memory device comprising:

a plurality of electrically rewritable nonvolatile memory cells connected in series; and

a select gate transistor connected in series to the series-connected memory cells, wherein a memory cell adjacent to said select gate transistor is a dummy cell being out of use for data storage.

2. The device according to claim 1, wherein said dummy cell is applied with a bias voltage being the same as a bias voltage for remaining memory cells during data erase.

3. The device according to claim 1, wherein said dummy cell is applied with a bias voltage being the same as a bias voltage of non-selected memory cells in data read and write events.

4. A nonvolatile semiconductor memory device comprising:

a plurality of electrically rewritable nonvolatile memory cells connected in series; and

a select gate transistor connected in series to the series-connected memory cells, wherein a memory cell adjacent to said select gate transistor is applied with a bias voltage different from a bias voltage of remaining memory cells during data erase.

5. The device according to claim 4, wherein data erase is for erasing all memory cells formed in a block in a well region at a time by holding control gates thereof at a low level while applying a high level of erase voltage to said well, and wherein a low level voltage being given to a control gate of the memory cell adjacent to said select gate transistor is set lower than that being applied to control gates of remaining memory cells.

6. The device according to claim 4, wherein during data writing for giving to a selected memory cell a write pulse voltage with a step-like incr as in voltage value, an

initial value of a write pulse voltage when the memory cell adjacent to said select gate transistor is selected is set at a different value from that when another memory cell is selected.

7. The device according to claim 6, wherein during said data write, the initial value of the write pulse voltage when the memory cell adjacent to said select gate transistor is selected is set higher than that when another memory cell is selected.

8. A nonvolatile semiconductor memory device comprising:

a plurality of NAND cell units each having a serial combination of electrically rewritable nonvolatile memory cells, a first select gate transistor inserted between one end of the series-connected memory cells and a bit line, and a second select gate transistor inserted between a remaining end of said series-connected memory cells and a source line; and

each said NAND cell unit including memory cells which are located adjacent to the first and second select gate transistors and which are dummy cells being out of use for data storage, wherein said dummy cells are applied with the same bias voltage as that of remaining memory cells during data erase and applied with the same bias voltage as that of non-selected memory cells in data read and write events.

9. A nonvolatile semiconductor memory device comprising:

a plurality of NAND cell units each having a serial combination of electrically rewritable nonvolatile memory cells, a first select gate transistor inserted between one end of the series-connected memory cells and a bit line, and a second select gate transistor inserted between a remaining end of said series-connected memory cells and a source line; and

said device having a data erase mode for erasing all memory c lls formed within a well region at a time by

holding control gates thereof at a low level while applying a high level of erase voltage to said well and a data write mode for giving to a selected memory cell a write pulse voltage with a step-like increase in voltage value, wherein

in said data erase mode, a low level voltage given to control gates of the memory cells adjacent to said first and second select gate transistors is set lower than that as given to control gates of remaining memory cells, and

in said data write mode, an initial value of a write pulse voltage when the memory cells adjacent to said first and second select gate transistors are selected is set higher than that when any one of the remaining memory cells is selected.